Amendments to the Claims

      This listing of claims will replace all prior versions and listings of claims in the application.

      1.   (currently amended) A wireless communications device, comprising:

      a wireless transceiver <u>being configured to wirelessly transmit voice and data</u>; and

      a processor coupled to the wireless transceiver, the processor having a memory <u>such that</u> <u>the memory is inside of the processor, the memory</u> comprising <u>at least six FIFO memory</u> <u>structures in which each FIFO memory structure comprises</u> a plurality of fragments<u>, the at least</u> <u>six FIFO memory structures comprising at least three pairs of FIFO memory structures, each</u> <u>FIFO memory structure pair storing a different type of data packet that is being transmitted and</u> <u>received, the memory comprising a respective single bit array corresponding to each FIFO</u> <u>memory structure, each fragment of associated FIFO memory structure being associated with a</u> <u>respective bit in the respective single bit array, the respective bit providing a status of the</u> <u>associated fragment, the memory comprising a respective second array correspond to each FIFO</u> <u>memory structure,</u> ~~and an~~ <u>the respective second</u> array <u>storing a respective link list and being</u> configured to control<u>, via the respective link list,</u> the sequence of memory fragments from which data is read.

      2.   (cancelled)

      3.   (currently amended) The wireless communications device of claim ~~2~~ <u>1</u> wherein the status indicated by the ~~second~~ <u>respective bit of the respective single bit</u> array for each of the memory fragments ~~comprises a bit to indicate~~ <u>is</u> whether ~~its~~ <u>the</u> respective memory fragment is empty.

      4.   (original) The wireless communications device of claim 1 wherein the processor

further comprises a read pointer configured to indicate the memory fragment from which the data is being read.

5. (original) The wireless communications device of claim 1 wherein each of the memory fragments comprises 64 bytes.

6. (original)   The wireless communications device of claim 1 wherein the memory fragments comprises 128 memory fragments.

7. (currently amended) The wireless communications device of claim 6 wherein the <u>respective second</u> array comprises a 128 element array.

8. (currently amended)   A processor comprising a memory <u>such that the memory is inside of the processor, the memory</u> having <u>at least six FIFO memory structures in which each FIFO memory structure comprises</u> a plurality of fragments<u>, the at least six FIFO memory structures comprising at least three pairs of FIFO memory structures, each FIFO memory structure pair storing a different type of data packet that is being transmitted and received, the memory comprising a respective single bit array corresponding to each FIFO memory structure, each fragment of associated FIFO memory structure being associated with a respective bit in the respective single bit array, the respective bit providing a status of the associated fragment, the memory comprising a respective second array correspond to each FIFO memory structure,</u> ~~and an~~ <u>the respective second</u> array <u>storing a respective link list and being</u> configured to control<u>, via the respective link list,</u> the sequence of memory fragments from which data is read.

9. (cancelled)

10. (currently amended) The processor of claim 9 wherein the status indicated by the ~~second~~ respective bit of the respective single bit array for each of the memory fragments ~~comprises a bit to indicate~~ is whether ~~its~~ the respective memory fragment is empty.

11. (original) The processor of claim 8 further comprising a read pointer configured to indicate the memory fragment from which the data is being read.

12. (original) The processor of claim 8 wherein each of the memory fragments comprises 64 bytes.

13. (original) The processor of claim 8 wherein the memory fragments comprises 128 memory fragments.

14. (currently amended) The processor of claim 13 wherein the respective second array comprises a 128 element array.

15. (new) The wireless communications device of claim 1 wherein hardware within the processor splits at least one FIFO memory structure into a second plurality of FIFO memory structures, each of the second plurality of FIFO memory structures serving a different device.

16. (new) The processor of claim 8 wherein hardware within the processor splits at least one FIFO memory structure into a second plurality of FIFO memory structures, each of the second plurality of FIFO memory structures serving a different device.

17. (new) The wireless communications device of claim 1 wherein a messaging mechanism reports an amount of memory available between a physical layer and a link control

layer.

18. (new) The processor of claim 8 wherein a messaging mechanism reports an amount of memory available between a physical layer and a link control layer.

19. (new) The wireless communications device of claim 1 wherein the processor pools memory among the at least six FIFO memory structures and dynamically allocates the memory among the at least six FIFO memory structures.

20. (new) The processor of claim 8 wherein the processor pools memory among the at least six FIFO memory structures and dynamically allocates the memory among the at least six FIFO memory structures.